

# DATA SHEET

**74LVC00A**

Quad 2-input NAND gate

Product specification  
Supersedes data of 1998 Apr 28

2002 Mar 05

## Quad 2-input NAND gate

## 74LVC00A

## FEATURES

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. 8-1A
- Specified from  $-40$  to  $+85$  °C and from  $-40$  to  $+125$  °C.

## DESCRIPTION

The 74LVC00A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall times.

The 74LVC00A provides the 2-input NAND function.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	2.1	ns
$C_I$	input capacitance		4.0	pF
$C_{PD}$	power dissipation capacitance per gate	$V_{CC} = 3.3$ V; notes 1 and 2	15	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_i = \text{GND to } V_{CC}$ .

## ORDERING INFORMATION

TYPE NUMBER	PACKAGES				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC00AD	$-40$ to $+125$ °C	14	SO	plastic	SOT108-1
74LVC00ADB	$-40$ to $+125$ °C	14	SSOP	plastic	SOT337-1
74LVC00APW	$-40$ to $+125$ °C	14	TSSOP	plastic	SOT402-1

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**FUNCTION TABLE**

See note 1.

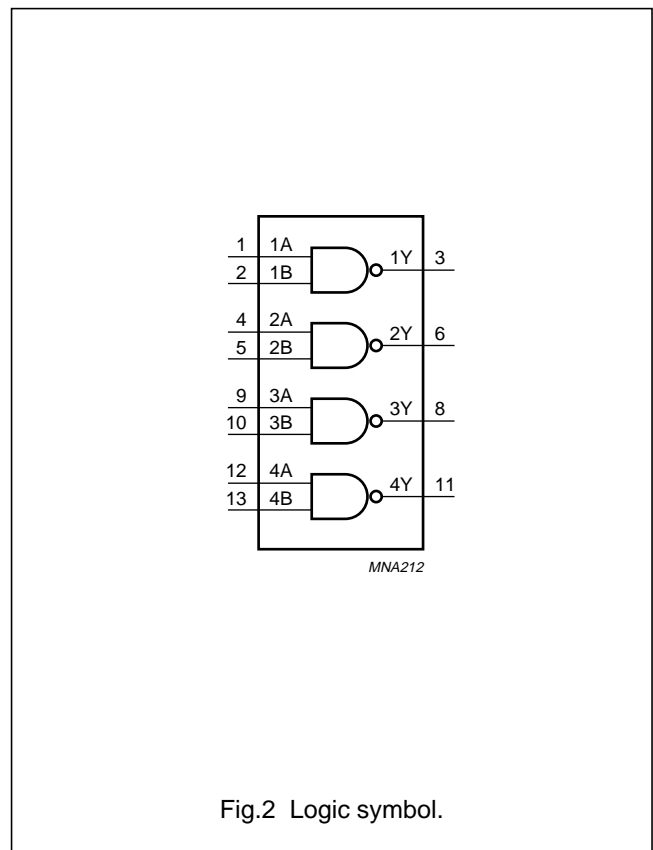
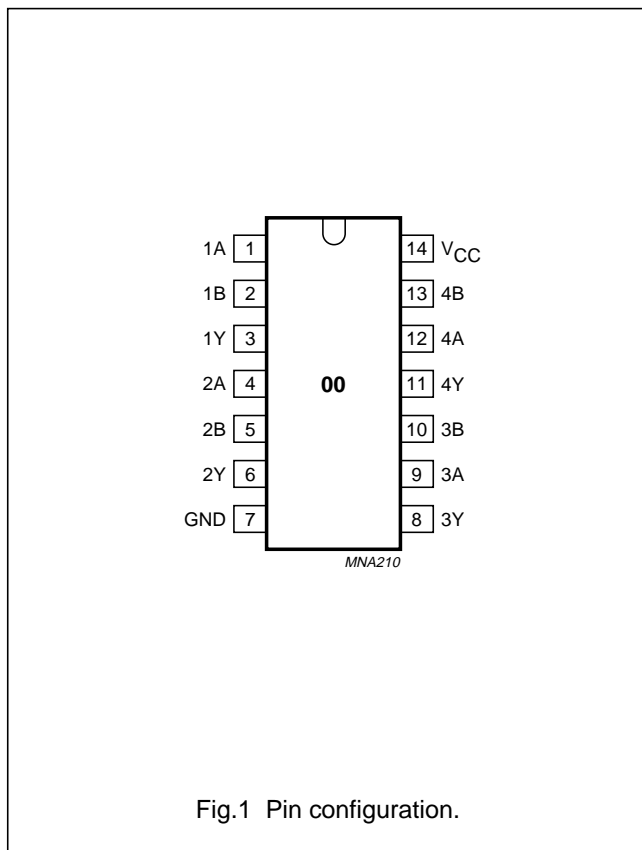
INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

**Note**

- 1. H = HIGH voltage level;  
L = LOW voltage level.

**PINNING**

PIN	SYMBOL	DESCRIPTION
1, 4, 9, 12	1A to 4A	data input
2, 5, 10, 13	1B to 4B	data input
3, 6, 8, 11	1Y to 4Y	data output
7	GND	ground (0 V)
14	V <sub>CC</sub>	supply voltage



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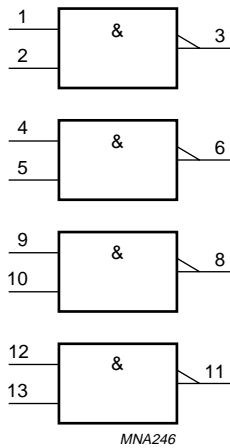


Fig.3 Logic symbol (IEEE/IEC).

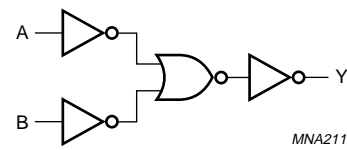


Fig.4 Logic diagram (one gate).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V <sub>I</sub>	input voltage		0	5.5	V
V <sub>O</sub>	output voltage		0	V <sub>CC</sub>	V
T <sub>amb</sub>	operating ambient temperature		-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 to 3.6 V	0	10	ns/V

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input diode current	$V_I < 0$	-	-50	mA
$V_I$	input voltage	note 1	-0.5	+6.5	V
$I_{OK}$	output diode current	$V_O > V_{CC}$ or $V_O < 0$	-	$\pm 50$	mA
$V_O$	output voltage	note 1	-0.5	$V_{CC} + 0.5$	V
$I_O$	output source or sink current	$V_O = 0$ to $V_{CC}$	-	$\pm 50$	mA
$I_{GND}, I_{CC}$	$V_{CC}$ or GND current		-	$\pm 100$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation per package				
	SO package	above 70 °C derate linearly with 8 mW/K	-	500	mW
	SSOP and TSSOP packages	above 60 °C derate linearly with 5.5 mW/K	-	500	mW

**Note**

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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**DC CHARACTERISTICS**

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		$T_{amb}$ (°C)					UNIT
		OTHER	$V_{CC}$ (V)	-40 to +85			-40 to +125		
				MIN.	TYP. <sup>(1)</sup>	MAX.	MIN.	MAX.	
$V_{IH}$	HIGH-level input voltage		1.2	$V_{CC}$	–	–	$V_{CC}$	–	V
			2.7 to 3.6	2.0	–	–	2.0	–	V
$V_{IL}$	LOW-level input voltage		1.2	–	–	GND	–	GND	V
			2.7 to 3.6	–	–	0.8	–	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	2.7 to 3.6	$V_{CC} - 0.2$	–	–	$V_{CC} - 0.3$	–	V
		$I_O = -100 \mu A$	2.7	$V_{CC} - 0.5$	–	–	$V_{CC} - 0.65$	–	V
		$I_O = -12 \text{ mA}$	3.0	$V_{CC} - 0.6$	–	–	$V_{CC} - 0.75$	–	V
		$I_O = -24 \text{ mA}$	3.0	$V_{CC} - 0.8$	–	–	$V_{CC} - 1$	–	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	2.7 to 3.6	–	–	0.2	–	0.3	V
		$I_O = 100 \mu A$	2.7	–	–	0.4	–	0.6	V
		$I_O = 24 \text{ mA}$	3.0	–	–	0.55	–	0.8	V
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND	3.6	–	$\pm 0.1$	$\pm 5$	–	$\pm 20$	$\mu A$
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	3.6	–	0.1	10	–	40	$\mu A$
$\Delta I_{CC}$	additional quiescent supply current per input pin	$V_I = V_{CC} - 0.6 \text{ V}$ ; $I_O = 0$	2.7 to 3.6	–	5	500	–	5000	$\mu A$

**Note**1. All typical values are at  $V_{CC} = 3.3 \text{ V}$  and  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

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**AC CHARACTERISTICS**

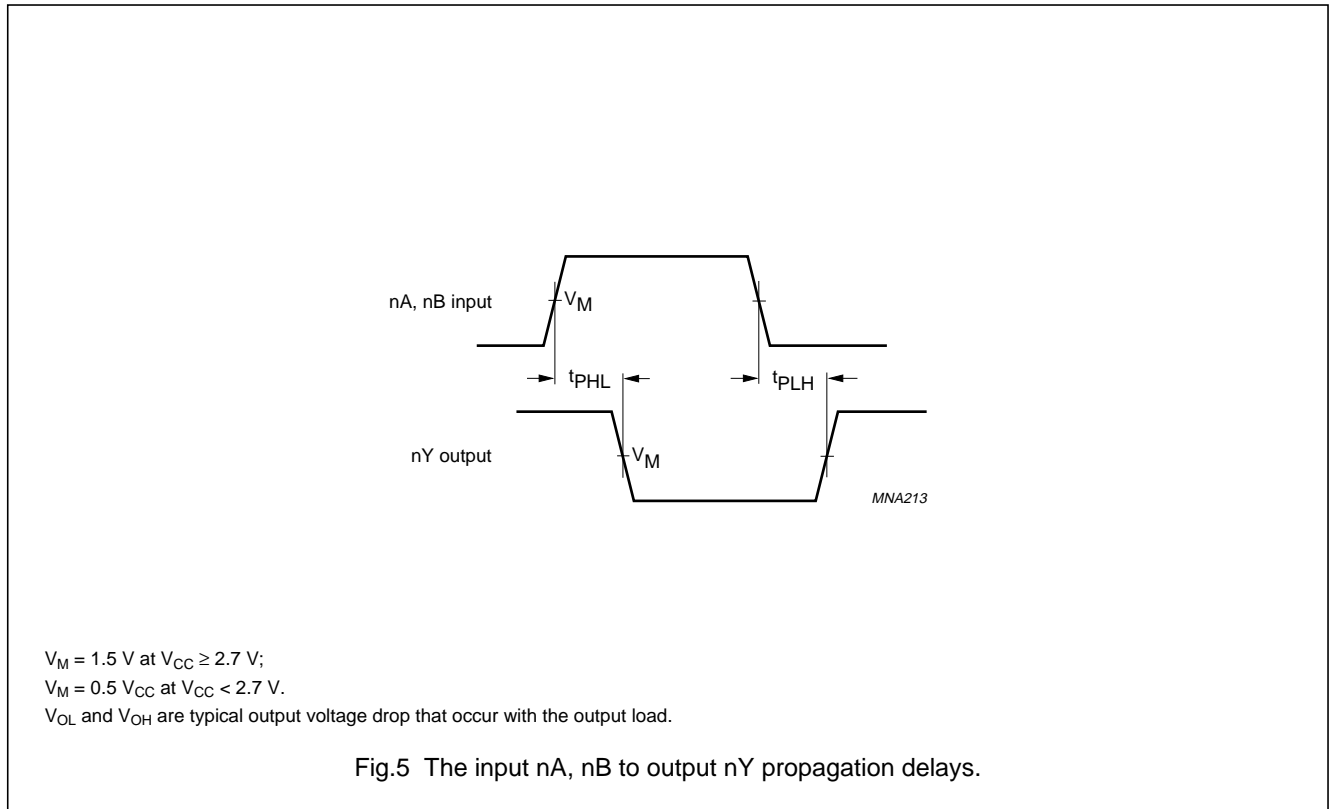
GND = 0 V;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	WAVEFORMS	$T_{amb}$ (°C)					UNIT
			-40 to +85			-40 to +125		
			MIN.	TYP. <sup>(1)</sup>	MAX.	MIN.	MAX.	
<b><math>V_{CC} = 1.2</math> V</b>								
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	see Figs 5 and 6	–	12	–	–	–	ns
<b><math>V_{CC} = 2.7</math> V</b>								
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	see Figs 5 and 6	1.5	2.4	5.1	1.5	6.5	ns
<b><math>V_{CC} = 3.0</math> to <math>3.6</math> V</b>								
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	see Figs 5 and 6	1.0	2.1	4.3	1.0	5.5	ns
$t_{sk(0)}$	skew	note 2	–	–	1.0	–	1.5	ns

**Notes**

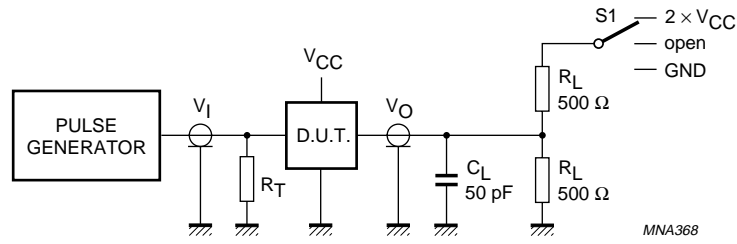
1. Typical values at  $V_{CC} = 3.3$  V.
2. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

**AC WAVEFORMS**



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$V_{CC}$	$V_I$	$t_{PLH}/t_{PHL}$
1.2 V	$V_{CC}$	open
2.7 V	2.7 V	open
3.0 to 3.6 V	2.7 V	open

Definitions for test circuits:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance (see Chapter "AC characteristics").

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig.6 Load circuitry for switching times.



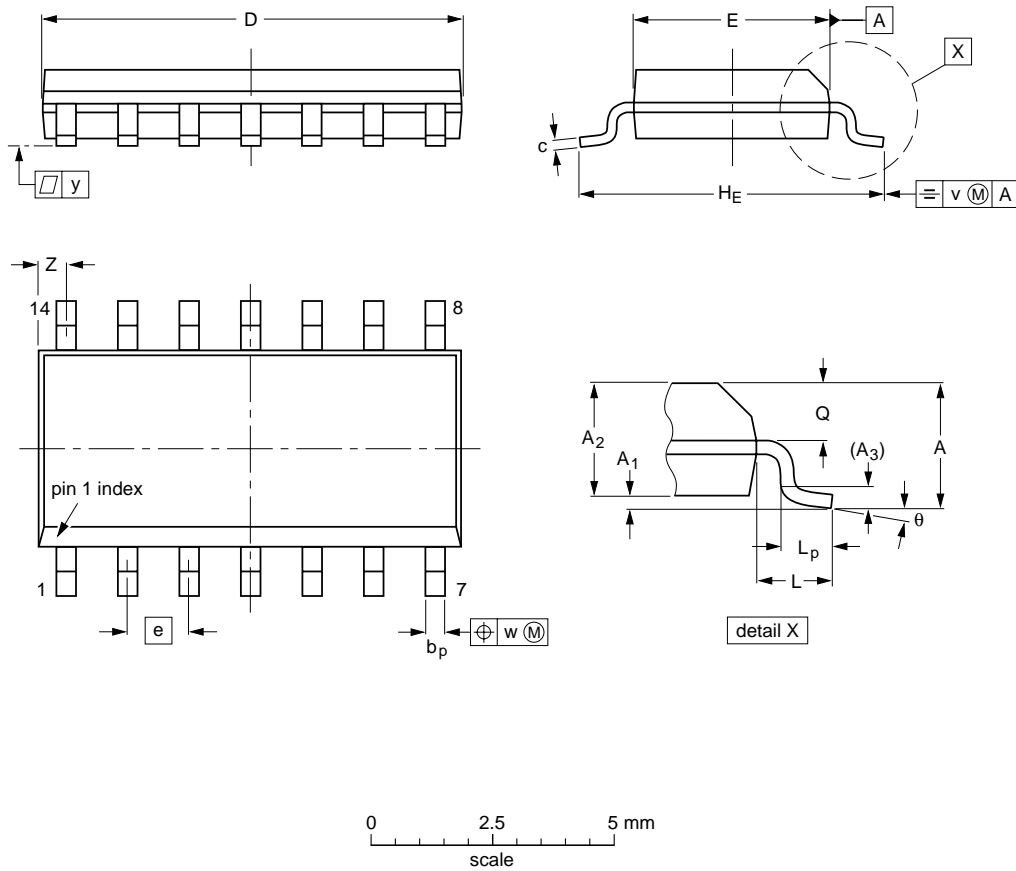
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PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

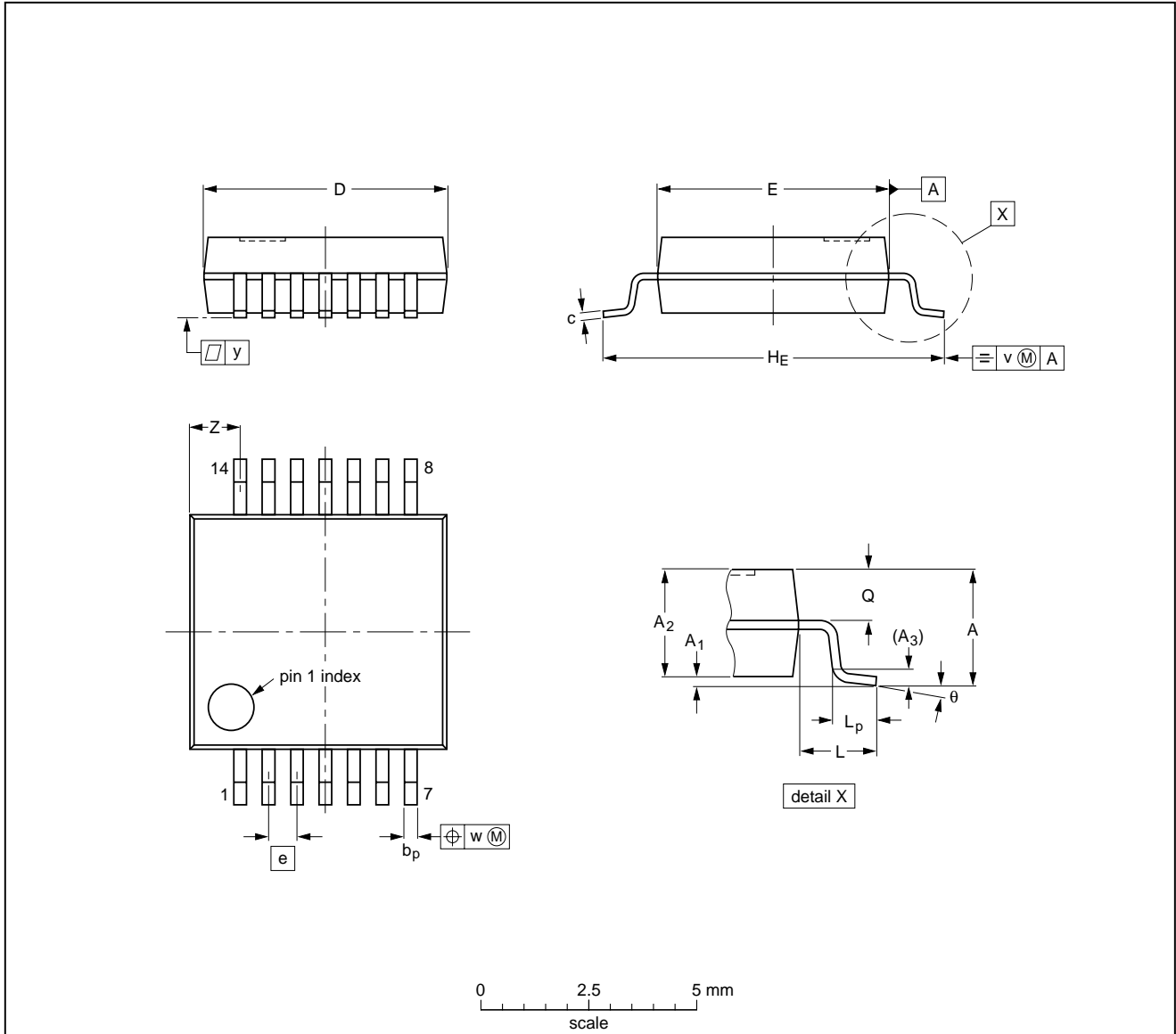
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				97-05-22 99-12-27

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

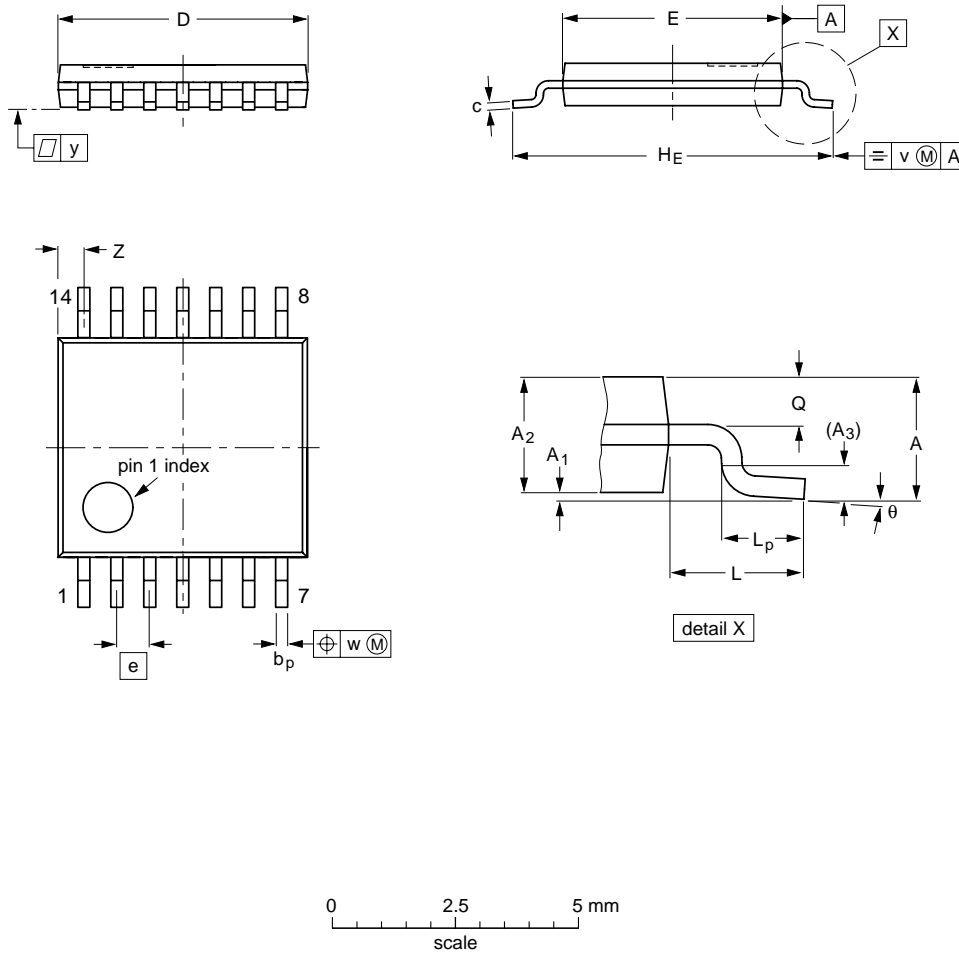
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150				<del>96-01-18</del> 99-12-27

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT402-1		MO-153			95-04-04 99-12-27

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### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

## Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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## DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
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Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

## Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Printed in The Netherlands

613508/03/pp16

Date of release: 2002 Mar 05

Document order number: 9397 750 09442

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